纳能微电子

IP name	IP description	Technology
USB2.0 host/device/OTG	>6000V HBM ESD	SMIC: 55nm 40nm 14nm 12nm
		TSMC: 40nm 28/22nm
		UMC: 55nm 28nm
		HLMC:40nm
USB3/PCIE2/SATA3/SGMII combo	One PHY to serve all three application	SMIC: 55nm 40nm 28nm 14/12nm
		TSMC: 28nm 22nm
		UMC: 55nm 28nm
		Samsung: 8nm
		HLMC:28nm
USB3.0/USB3.1 type-C PHY(Combo eDP TX)	Type-C application	SMIC: 14nm
		TSMC: 55nm
		UMC: 55nm
PCIE Gen3 PHY	Up to 8Gbps, 16lanes	SMIC 14nm
		UMC: 55nm 28nm
		GF: 22nm
PCIE Gen4 PHY	16G, 4 lanes	UMC: 28nm
SAS 12G PHY	12G, 4 lanes	SMIC: 28nm
		UMC: 28nm
		TSMC： 28nm
JESD204B PHY	Multi-lane up to 12.5Gbps	SMIC: 14nm
		TSMC: 55nm 28nm
		UMC: 55nm 28nm
or XAUI/RapidIO and other general SERDES a	1G – 12.5G general purpose SERDES	SMIC 55nm 40nm 14nm
		TSMC: 28nm
		UMC:28nm
VByOne/LVDS combo TX PHY	Up to 4Gbps, 24 lanes	SMIC: 40nm
		GF: 22nm FDSOI
VByOne/MIPI/LVDS combo TX PHY	3-in-1 combo PHY for video application	SMIC: 40nm
MIPI-DSI/CSI PHY TSMC: 22nm/		TSMC: 22nm/28nm
VByOne/eDP/P2P combo TX PHY		TSMC: 22nm/28nm
LVDS IO/PHY		SMIC: 55nm 40nm 14nm
		TSMC:22nm
		UMC: 55nm
High performance PLL	1G-3.5GHz	SMIC: 14nm
		TSMC:28nm/22nm
3.3V tolerance GPIO library		SMIC: 14nm
LDO IP	5V-3.3V input/3.3V-0.9V out	UMC: 55nm
DC-DC IP	5V -3.3V input/1.5-0.9 outpu	UMC: 55nm